WHAT IS CLAIMED IS:

1. A method for recovering a clock signal from an input data signal in a telecommunications system, the method comprising the steps of:

- comparing the input data signal with a recovered clock signal in order to control said recovered clock signal generation; and

- generating a plurality of delayed clock signals, obtained by multi-delaying at least a reference signal, said delayed clock signals being phase-shifted with respect to each other,

wherein said delayed clock signals show a phase shift with respect to each other, that is nominally constant in time, and wherein it further comprises the step of selecting the recovered clock signal among said delayed clock signals.

2. Method according to claim 1, wherein it further comprises the step of employing a number of delayed signals, such that the sum of the shifts associated to such delayed signals covers the bit period of the input data signal.

3. Method according to claim 2, wherein it further comprises the step of dynamically changing the number of delayed signals by comparing the bit period with the shift sum.

4. Method according to claim 3, wherein the shift between each adjacent pair of delayed signals is nominally equal.

5. Method according to claim 3, wherein it comprises the step of obtaining said plurality of delayed clock signals by multi-delaying a single sole reference signal.

6. Method according to claim 4, wherein it further comprises the step of selecting a first recovery signal and a second recovery signal before selecting the recovery clock signal.

7. Method according to claim 5, wherein it further comprises the step of switching between said first recovery signal and said second recovery signal for selecting the recovery clock signal.

8. Method according to claim 5, wherein it comprises the step of shifting the first recovery signal and the second recovery signal by one time interval.

9. Method according to claim 6, wherein it comprises the step of shifting the first recovery signal and the second recovery signal by one time interval.

10. Method according to claim 5, wherein it further comprises the step of providing enabling signals for activating switching between said first recovery signal and said second recovery signal.

11. Method according to any of claims 1, wherein it further comprises the step of comparing the input data signal with the recovered clock signal, by using the comparison of several phases of the input data signal and/or of the recovered clock signal, so as to obtain a plurality of samples for each sampling cycle.

12. Method according to claim 10, wherein it further comprises the step of filtering the output of the comparison operation.

13. Circuit for recovering a clock signal from an input data signal in a telecommunications network, the circuit comprising a phase comparator comparing the input data signal phase and the recovery clock signal phase for supplying a phase information, which controls generating means of said recovery clock signal, wherein said generating means comprise a delay line having a plurality of taps for generating a plurality of delayed signals.

14. Circuit according to claim 13, wherein said generating means comprise selection means of the recovered clock signal.

15. Circuit according to claim 13, wherein said selection means comprise a first selection block for selecting a first recovery signal and a second recovery signal from the plurality of delayed signals, and further comprise a second switch block for switching between said first recovery signal and said second recovery signal.

16. Circuit according to claim 14, wherein said selection means comprise, moreover, a control logics driving the first selection block and the second switch block according to the phase information supplied by the phase comparator.

17. Circuit according to claim 15, wherein said control logics comprises a filter for filtering the phase information.

18. Circuit according to claim 15, wherein said control logics comprises a logic machine issuing selection signals and enable signals according to the phase information.